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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PARIKH, KALPIT	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,456	OMATHUNA, PADRAIG	
	Examiner	Art Unit	
	KALPIT PARIKH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant detailed action is in response to Applicant's submission filed on 17 May 2010.

I. APPLICATION INFORMATION

Application No. 10/538456 has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

II. REJECTIONS NOT BASED ON PRIOR ART

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of integrated circuits (ICs) disposed on a substrate and communicatively coupled to one another through test circuitry that provides debugging capabilities, and transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

III. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **CLAIMS 1-5 AND 7-9** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and May (US Pat No. 7343483).

   As per claim 1, Yamada discloses a method of transferring programming instructions from a first memory disposed on a substrate, to a plurality of integrated circuits (ICs), comprising:

- a first one of the plurality of ICs (see Yamada FIG 1: 1 MASTER CPU) accessing the first memory (see Yamada FIG 6: S2), retrieving a first set of programming instructions, and storing the first set of programming instructions within the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 32-46); and
- the first one of the plurality of ICs accessing the first memory, retrieving a second set of programming instructions, and transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose the memory and the plurality of integrated circuit (ICs) are disposed on the substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamada and Stancil does not expressly disclose

- communicatively coupled to one another through test circuitry that provides debugging capabilities,
- transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs.

In the same filed of endeavor May discloses

- communicatively coupled to one another through test circuitry that provides debugging capabilities (see May FIG 2: 240),

  [The embedded controller is construed as a first integrated circuit and the PLD array is construed as the second integrated circuit.]

- transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs (see May COL 3 LINES 24-41).

It would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by May.

The suggestion/motivation for doing so would have been for the benefit of a test interface (see May FIG 2: 'PLD TEST INTERFACE' and COL 3 LINES 40-45).

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by May for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 2, Yamada in view of Stancil and May disclose the method of Claim 1,

- wherein the first and second ones of the plurality of ICs each comprise a processor capable of executing, respectively, the first and second sets of programming instructions (see Yamada FIG 6: S3, S5: 'PROGRAM DATA') and
- further including the step of debugging the plurality of ICs using the test circuitry by operating the test circuitry in a test mode (see May FIG 2: PLD TEST INTERFACE) and
- wherein each of the steps of accessing retrieving, storing and transmitting is implemented when the test circuitry is in a mode other than the test mode (see May COL 3 LINES 24-41).

  [May discloses JTAG which is understood to include a test mode as recited in the claims (see May FIG 2: PLD JTAG).]

As per claim 3, Yamada in view of Stancil and May disclose the method of Claim 2, further comprising

- the first one of the plurality of ICs executing at least a portion of the first set of programming instructions (see Yamada COL 3 LINES 45-55);
- in a test mode, operating the test circuitry using control signals from a source external to the substrate (see May FIG 2: PLD TEST INTERFACE) and
- in a mode other than the test mode, operating the test circuitry using control signals generated on the substrate (see May COL 3 LINES 24-41).

  [May discloses JTAG which is understood to include a test mode as recited in the claims (see May FIG 2: PLD JTAG).]

As per claim 4, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein executing at least a portion of the first set of programming instructions occurs prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see May COL 3 LINES 42-52).

As per claim 5, Yamada in view of Stancil and May disclose the method of Claim 2,

- further comprising the first one of the plurality of ICs accessing the first memory, retrieving a first set of data, and storing the first set of data within the first one of the plurality of ICs; and the first one of the plurality of ICs accessing the first memory, retrieving a second set of data, and transmitting the second set of data to a second one of the plurality of ICs (see Yamada FIG 6: S3, S5).

As per claim 7, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein transmitting comprises serially shifting data out from the first integrated circuit and concurrently shitting data in to the second integrated circuit (see Yamada FIG 6: S5 "SERIALLY TRANSFER").

As per claim 8, Yamada in view of Stancil and May disclose the method of Claim 7,

- further comprising transmitting control information from the first integrated circuit to the second integrated circuit prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S4).

As per claim 9, Yamada in view of Stancil and May disclose the method of Claim 8,

- wherein the control information directs the second one of the plurality of ICs to receive a subsequent transmission of programming instructions (see Yamada FIG 6: S5).

3. **CLAIMS 6** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and May (US Pat No. 7343483) as applied to claim 3 above and further in view of Sun Microelectronics (NPL: Introduction to JTAG Boundary Scan).

As per claim 6, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein the substrate comprises a printed circuit board (see Stancil COL 2 LINE 25: "motherboard"), and

However, Yamada in view of Stancil and May does not expressly disclose

- the test circuitry of each of the plurality of ICs has an input for a test mode signal and a clock that is common to each of the plurality of ICs.

In the same field of endeavor Sun Microelectronics discloses

- the test circuitry of each of the plurality of ICs has an input for a test mode signal (see Sun Microelectronics PAGE 3 2nd Paragraph) and a clock that is common to each of the plurality of ICs (see Sun Microelectronics PAGE 6 FIG 3: TCK).

It would have been obvious to modify Yamada in view of Stancil and May to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

4. **CLAIMS 10-14** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Sun Microelectronics (NPL: Introduction to JTAG Boundary Scan).

   As per claim 10, Yamada discloses in a system including a plurality of integrated circuits (ICs), each IC having a memory for storing at least programming instructions, and a processor coupled to the memory for executing programming instructions stored in the memory; the system further including a single non-volatile memory disposed on the printed circuit board and coupled for memory access to only a first one of the plurality of ICs, a method of downloading code from the single non-volatile memory to each of the plurality of ICs, comprising:

   - receiving, at a first one of the plurality of ICs, a first set of data from the single non-volatile memory; storing the first set of data in the memory of the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 28-46);
   - receiving, at the first one of the plurality of ICs, a second set of data from the single non-volatile memory; transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and storing the second set of data in the memory of the second one of

the plurality of ICs; wherein the first and second sets of data comprise program code (see Yamada FIG 6: S5 and COL 3 LINES 28-46).

However, Yamada does not expressly disclose the plurality of ICs disposed on a printed circuit board.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamada and Stancil does not expressly disclose

- test circuitry for providing debugging functionality
- transmitting, using the debugging circuitry, the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and

In the same filed of endeavor Sun Microelectronics discloses

- test circuitry for providing debugging functionality (see Sun Microelectronics PAGE 2 FIG 1: Input Boundary Cell, Output Boundary Cell and PAGE 6 FIG 3),
- transmitting, using the debugging circuitry, the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and (see Sun Microelectronics PAGE 2 FIG 1: Input Boundary Cell, Output Boundary Cell and PAGE 6 FIG 3).

  [Placing the boundary scan cells at the input and output would necessarily entail the data be sent via the boundary scan cells.]

It would have been obvious to modify Yamada in view of Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 11, Yamada in view of Stancil and Sun Microelectronics discloses the method of Claim 10,

- further comprising: executing, in the first IC, at least a portion of the code in the program first set of data (see FIG 6: S6);
- receiving, at the first one of the plurality of ICs, a third set of data from the single non-volatile memory; transmitting the third set of data from the first one of the plurality of ICs to a third one of the plurality of ICs; and storing the third set of data in the memory of the third one of the plurality of ICs (see Stancil FIG 2: 114, 116, 118);

As per claim 12. Yamada in view of Stancil and Sun Microelectronics disclose the method of Claim 10,

- wherein transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs comprises serially shifting data out of the first one of the plurality of ICs via an output terminal; wherein the output terminal is coupled to an input terminal of the second one of the plurality of ICs, the input terminal coupled to circuitry within the second one of the plurality of ICs that is adapted to receive serial data (see Yamada FIG 6: S5 SERIALLY).

As per claim 13, Yamada in view of Stancil and Sun Microelectronics disclose the method of Claim 12,

- further comprising placing the test circuitry in a test mode (see Sun Microelectronics PAGE 3 Paragraph 2) and
- providing transmitting control information from the first one of the plurality of ICs to the second one of the plurality of ICs prior to transmitting the second set of data (see Yamada FIG 6: S4).

As per claim 14, Yamada in view of Stancil and May disclose the method of claim 13.

- wherein the control information is transmitted in accordance with a JTAG standard of communication (see Sun Microelectronics Page 3: "JTAG Basics").

5. **CLAIMS 15-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Sun Microelectronics (NPL Introduction to JTAG Boundary Scan).

As per claim 15, Yamada discloses an electronic product, comprising: a first integrated circuit having a first processor (see Yamada FIG 1: 1), a first internal memory (see Yamada FIG 1: 3), a first serial communication interface (see Yamada FIG 1: "SERIAL COMMUNICATION"), and an external memory interface (see Yamada FIG 1: 4); an external memory coupled to the external memory interface (see FIG 1: 5 MEMORY CARD); a second integrated circuit having second processor (see FIG 1: 6), a second internal memory (see FIG 1: 8), and a second serial communication interface, the second serial communication interface being coupled to the first serial communication interface (see FIG 1: "SERIAL COMMUNICATION");

- wherein the first test circuit and the second test circuit are configured communicate code images in another mode (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamda and Stancil does not expressly disclose

- a first test circuit
- a second test circuit
- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode.

In the same field of endeavor Sun Microelectronics discloses

- a first test circuit (see Sun Microelectronics PAGE 3 FIG 1 Input Boundary Cell and PAGE 6 FIG 3)
- a second test circuit (see Sun Microelectronics PAGE 3 FIG 1 Input Boundary Cell and PAGE 6 FIG 3)
- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode (see Sun Microelectronics PAGE 3 2nd Paragraph).

It would have been obvious to modify Yamada in view of Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 16, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of claim 15,

- wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image (see Yamada FIG 6: S3), the second processor is coupled to the second internal memory, the second internal memory is adapted to receive a second code image (see Yamada FIG 6: S5), and the external memory is a non-volatile memory encoded with the first and second code images (see Yamada COL 2 LINES 50-57).

As per claim 17, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of claim 16,

- wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different (see Yamada COL 3 LINES 24-45).

As per claim 18, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of Claim 17, further comprising

- a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image (see Stancil FIG 2: 114, 116, 118).

  [Stancil discloses configuring plural processing devices using a single EEPROM.]

6. **CLAIMS 15-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Chang (US Pat No. 6484273).

   As per claim 15, Yamada discloses an electronic product, comprising: a first integrated circuit having a first processor (see Yamada FIG 1: 1), a first internal memory (see Yamada FIG 1: 3), a first serial communication interface (see Yamada FIG 1: "SERIAL COMMUNICATION"), and an external memory interface (see Yamada FIG 1: 4); an external memory coupled to the external memory interface (see FIG 1: 5 MEMORY CARD); a second integrated circuit having second processor (see FIG 1: 6), a second internal memory (see FIG 1: 8), and a second serial communication interface, the second serial communication interface being coupled to the first serial communication interface (see FIG 1: "SERIAL COMMUNICATION");

   - wherein the first test circuit and the second test circuit are configured communicate code images in another mode (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

   However, Yamada does not expressly disclose wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate.

   In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

   It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamda and Stancil does not expressly disclose

- a first test circuit
- a second test circuit
- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode.

In the same field of endeavor Chang discloses an integrated circuit (see Chang FIG 1) including a test circuit (see Chang FIG 2: 54), wherein the test circuit is configured and arranged to communicate debugging information in a test mode (see COL 2 LINES 58-65) and to communicate code images in another mode (see Chang COL 2 LINES 1-10).

It would have been obvious to modify each of the first and second integrated circuits as taught by Yamda and Stancil to include a test circuit as taught by Chang.

The suggestion/motivation for doing so would have been for the benefit of a non-intrusive development and debug technology (see Chang COL 1 LINES 35-45).

Therefore it would have been obvious to modify Yamada and Stancil to implement a test circuit as taught by Chang for the benefit of debugging technology to arrive at the invention as specified in the claims.

As per claim 16, Yamada in view of Stancil and Chang disclose the electronic product of claim 15,

- wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image (see Yamada FIG 6: S3), the second processor is coupled

to the second internal memory, the second internal memory is adapted to receive a second code image (see FIG 6: S5), and the external memory is a non-volatile memory encoded with the first and second code images (see COL 2 LINES 50-57).

As per claim 17, Yamada in view of Stancil and Chang disclose the electronic product of claim 16,

- wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different (see COL 3 LINES 24-45).

As per claim 18, Yamada in view of Stancil and Chang disclose the electronic product of Claim 17, further comprising

- a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image (see Stancil FIG 2: 114, 116, 118).

[Stancil discloses configuring plural processing devices using a single EEPROM.]

IV. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Applicants' arguments filed 17 May 2010 have been fully considered.

Examiner notes the instant office action clarifies the section relied upon to reject claims 2 and 3.

RESPONSE TO AMENDMENTS/ARGUMENTS

1st ARGUMENT:

Applicant traverses the § 103(a) rejections of claims 1-9 because the Office Action has failed to provide a proper reason to combine the '639 reference, the '584 reference and the '483 reference to form the asserted hypothetical combination, contrary to the requirements § 2143.01. The Office Action on page 4 asserts that the motivation to combine the references would be "for the benefit of a test interface and the use of an industry standard protocol." However, the Office Action fails to explain what part of the '639 reference is being tested, or if the PLD controller of the '483 reference would be a proper testing protocol for the signal between the master CPU and the slave CPU of the '639 reference.

Examiner respectfully disagrees. Motivation to implement a test interface is self-evident, namely to provide debugging capability. The references are understood to teach the limitation to the extent required by the claim language. The claim does not specify the portion of the device that is being tested, and it is unclear why the absence of a description pertaining to the portion of the device being tested in the reference is relevant. The testing circuitry is understood to test the device. Examiner clarifies the '639 teaches the JTAG protocol, which is understood to test signals from CPUs as taught by the '483 reference.

In response to applicant's argument that it is unclear if the PLD controller of the '483 reference would be a proper testing protocol for the signal between the master CPU and the slave CPU of the '639 reference, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

2nd ARGUMENT:

> Further, one of skill in the art would understand that CPUs of the '639 reference already include internal self-testing (software based) functionality as well as testing functionality from Figure 6 (step S4) and Figure 7 (step S12). Also, CPUs are known to be testable by way of the functions they perform (e.g., communications between the master and slave CPUs), and the serial line between the master and slave CPUs would not be tested by a PLD Device controller because it is not a programmable logic device. Moreover, the addition of a PLD controller as asserted would inherently increase the likelihood of the circuit not operating properly and require more testing of the device. Accordingly, the Office Action has failed to provide a proper reason for the proposed combination of references. The § 103(a) rejection of claims 1-9 must therefore be withdrawn.

Examiner respectfully disagrees. Examiner notes even if step S4 and step S12 are construed to disclose testing functionality, no portion of the '639 reference disclose testing circuitry that provides debugging capabilities as recited in the claims. The '483 reference discloses implementing JTAG, which is understood to provide debugging capabilities. Examiner further notes testing functionality is not

understood to be an inherent feature of CPUs at least because not every CPU is understood to require testing functionality to carry out its intended functionality. While Examiner does not dispute that CPUs may be tested by way of the functions they perform, such a method of testing is not understood to render all other methods of testing superfluous. A person of skill in the art would recognize testing CPUs by the function they perform is necessarily limited in scope, and other methods of testing may be required to perform debugging as evidence by the existence of JTAG.

The suggestion that the addition of the PLD controller would increase the likelihood of the circuit not operating properly is mere conjecture. Applicants' representative provides no facts or evidence to support the conclusion. Notwithstanding the fact that a PLD controller is necessary to program a PLD array as taught by the '483, there is simply no evidence cited or present in the prior art of record to conclude implementing a PLD controller and array increases likelihood of failure.

3rd ARGUMENT:

> Applicant submits that the combination would render the invention inoperable because "the master CPU checks whether or not the slave CPU is ready for serial reception in step 4." Col. 3:39-41. If the PLD controller was placed between the master and slave CPUs of the '639 reference, the master CPU would be unable to check whether the slave CPU was ready for serial reception. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Examiner respectfully disagrees. In response to applicant's argument that the PLD controller would render the invention inoperable, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

It is further unclear on what basis Applicants' representative is suggesting the PLD controller would interfere with communications between the master CPU and the slave CPU as taught by the '639 reference. Rather as per the '483 reference the PLD controller facilitates communications between an

embedded controller (master CPU) and a PLD array (slave CPU) (see May COL 3 LINES 25-45: "a second configuration data section is sent to PLD array 220, via PLD controller 240."). Applicants' representative provides no evidence to support the conclusion the PLD controller would render the invention inoperable.

4th ARGUMENT:

> Further, the rejection of claims 1-9 has engaged in improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statement at page 4 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to communicatively couple the first and second integrated circuits through test circuitry as taught by May for the benefit of a test interface to arrive at the invention as specified in the claims." Thus, the alleged motivation is "to arrive at Applicant's invention," which is per se improper. Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 1-9 is improper and should be withdrawn.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Examiner disputes the motivation to combine came from Applicants' claims, as Applicants' representative previously argues in the 3rd argument, it is well known to implement testing circuitry for CPUs.

Examiner further notes Applicants' state the testing circuitry so relied upon to claim novelty is admitted prior art (see Specification PAGE 3 LINES 5-15: "by using existing communications interface on each of the SoCs that is normally used for system debugging operations").

5th ARGUMENT:

> Applicant traverses the § 103(a) rejections of claims 10-18 because the Office Action has failed to provide a proper reason to combine the '639 reference, the '584 reference and the Sun reference to form the asserted hypothetical combination, contrary to the requirements § 2143.01. The Office Action, on pages 9 and 12, asserts that the motivation to combine the references would be "for the benefit of a test interface and the use of an industry standard protocol."

> However, the Office Action fails to explain what part of the '639 reference is being tested or how the JTAG circuit of the Sun reference would (or could) be a proper testing protocol for the signal between the master CPU and the slave CPU of the '639 reference.

Examiner respectfully disagrees. Motivation to implement a test interface is self-evident, namely to provide debugging capability. The references are understood to teach the limitation to the extent required by the claim language. The claim does not specify the portion of the device that is being tested, and it is unclear why the absence of a description pertaining to the portion of the device being tested in the reference is relevant. The testing circuitry is understood to test the device.

Examiner notes the Sun reference states 'Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via softwaree control. (see PAGE 2: "What is Boundary Scan?").'

6th ARGUMENT:

> Further, one of skill in the art would understand that CPUs of the '639 reference already include testing functionality from Figure 6 (step S4) and Figure 7 (step S12). Also, the addition of a JTAG circuit as asserted would inherently increase the likelihood of the circuit not operating properly and require more testing of the device. Accordingly, the Office Action has failed to provide a proper reason for the proposed combination of references. The § 103 (a) rejection of claims 10-18 must therefore be withdrawn.

Examiner respectfully disagrees. Examiner notes even if step S4 and step S12 are construed to disclose testing functionality, no portion of the '639 reference disclose testing circuitry that provides debugging capabilities as recited in the claims. The '483 reference discloses implementing JTAG, which is understood to provide debugging capabilities. Examiner further notes testing functionality is not understood to be an inherent feature of CPUs at least because not every CPU is understood to require testing functionality to carry out its intended functionality. While Examiner does not dispute that CPUs may be tested by way of the functions they perform, such a method of testing is not understood to render all other methods of testing superfluous. A person of skill in the art would recognize testing CPUs by the function they perform is necessarily limited in scope, and other methods of testing may be required to perform debugging as evidence by the existence of JTAG.

The suggestion that the addition of a JTAG circuit as asserted would inherently increase the likelihood of the circuit not operating properly and require more testing of the device appears to be mere conjecture at least because no evidence has been cited to support such a conclusion. Irrespective of any added complexity, the Sun reference clearly discloses the motivation for implementing boundary scan testing method.

7th ARGUMENT:

> Applicant further traverses the § 103(a) rejection of claims 10-18 because one of skill in the art would not be motivated to combine the references as claimed. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('639) reference - the rationale being that the prior art teaches away from such a modification. See KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the combination would render the invention inoperable because "the master CPU checks whether or not the slave CPU is ready for serial reception in step 4." Col. 3:39-41. If the JTAG circuit was placed between the master and slave CPUs of the '639 reference, the master CPU would be unable to check whether the slave CPU was ready for serial reception. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Examiner respectfully disagrees. Examiner initially notes it is unclear on what basis Applicants' representative is suggesting the inclusion of the JTAG circuit would render the master CPU incapable of checking the slave CPU. JTAG is understood to be a non-intrusive testing methodology, and therefore would not interfere with the normal operation of the master CPU. Indeed the Sun reference discloses a bypass instruction that would bypass the boundary scan chain (See Sun Microsystems PAGE 4: Required Instructions: 3. BYPASS Instruction).

8th ARGUMENT:

> Again, with this rejection of claims 10-18, the Office Action has engaged m improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statements at pages 9 and 12 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to communicatively couple the first and second integrated circuits through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims." Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 10-18 is improper and should be withdrawn.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Examiner disputes the motivation to combine came from Applicants' claims, as Applicants' representative previously argues in the 3rd argument, it is well known to implement testing circuitry for CPUs.

Examiner further notes Applicants' state the testing circuitry so relied upon to claim novelty is admitted prior art (see Specification PAGE 3 LINES 5-15: "by using existing communications interface on each of the SoCs that is normally used for system debugging operations").

9th ARGUMENT:

> Applicant further traverses the § 103 (a) rejection of claims 15-18 over the combination of the '639 reference and the '273 and '584 references because the Office Action has failed to provide a proper reason to combine the references as asserted in the hypothetical combination, contrary to the requirements of M.P.E.P. § 2143.01. The Office Action asserts the motivation would be "for the benefit of a non-intrusive development and debug technology". However, the Office Action again fails to provide any indication of what from the primary '639 reference is being tested, nor has the Office

Examiner respectfully disagrees. Motivation to implement a test interface is self-evident, namely to provide debugging capability as disclosed by the '584 reference. The references are understood to teach the limitation to the extent required by the claim language. The claim does not specify the portion of the device that is being tested, and it is unclear why the absence of a description pertaining to the portion of the device being tested in the reference is relevant. The testing circuitry is understood to test the device.

10th ARGUMENT:

> Action provided any explanation as to why master and slave CPUs coupled through a serial connection for the purposes outlined in the '639 reference require debugging. The Office Action fails to explain why an integrated JTAG is necessary when no bus is present, but rather a simple wire connecting the two CPUs. Accordingly, the § 103(a) rejection is improper and should be withdrawn.

The wire connecting the two CPUs is understood to be a bus at least because the wire is used to communicate between the two CPUs. The 584' reference is relied upon to provide the motivation for implementing an integrated JTAG namely in-circuit debugging. The 584' reference clearly discloses there is a need in the art for implementing debug and development tools (see Chang COL 1 LINES 10-25).

11th ARGUMENT:

> Applicant further traverses the § 103(a) rejection of claims 15-18 over the combination of the '639 reference and the '273 and '584 references because the Office Action has engaged in improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statement at page 15 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to implement a test circuit as taught by [the '273 reference] for the benefit of debugging technology to arrive at the invention as specified in the claims." As discussed above, the alleged motivation is "to arrive at Applicant's invention," which is per se improper. Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 15-18 is improper and should be withdrawn.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Examiner disputes the motivation to combine came from Applicants' claims, as Applicants' representative previously argues in the 3rd argument, it is well known to implement testing circuitry for CPUs.

Examiner further notes Applicants' state the testing circuitry so relied upon to claim novelty is admitted prior art (see Specification PAGE 3 LINES 5-15: "by using existing communications interface on each of the SoCs that is normally used for system debugging operations").

12th ARGUMENT:

> In response to the objection to the drawings, Applicant submits that the objection is improper and not required under 37 C.F.R. 1.83 (a). In support of Applicant's position reference is made to 35 USC §113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be

> patented." The Office Action has not indicated why one skilled in the art would not be able to understand the claimed invention. In addition, M.P.E.P. § 601.01(f) indicates that it has been PTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 USC § 113. Since most of the claims in the current application are method claims, Applicant has complied with M.P.E.P. § 601.01(f).

Examiner initially notes the objection was made under 37 C.F.R. 1.83 (a). Arguing the drawings are compliant with 35 USC 113 does not address the deficiency under 37 C.F.R. 1.83 (a).

37 C.F.R. 1.83 (a) states in part:

> The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box). In addition, tables and sequence listings that are included in the specification are, except for applications filed under 35 U.S.C. 371, not permitted to be included in the drawings.

The drawings do not show every feature of the invention specified in the claims. The drawing objection may be overcome by illustrating the transferring via the testing circuitry as recited in the claims.

13th ARGUMENT:

> Notwithstanding M.P.E.P. § 601.01(f), Applicant submits that the claimed feature is adequately described by the reference to the numerical labels shown in Figures 4-8. For example, Figure 4 shows a high level schematic of a SoC, with testing circuitry 410 connected to bus 420. Further, the description of Figure 5 indicates that pathway 518 is connected to the test data output terminal of one SoC and test data input terminal of a second SoC. Accordingly the drawings depict IC circuits "communicatively coupled to one another through test circuitry that provides debugging capabilities, and transmitting, using the test circuitry, the second set of programming instructions." Office Action page 2. Therefore, Applicant requests the drawing objection be withdrawn.

Examiner respectfully disagrees. While FIG 4 illustrates testing circuitry 410, no portion of the drawing illustrates the transferring is performed via the testing circuitry as recited in the claims. FIG 4 further does not illustrate a second IC as recited in claim 1, and therefore cannot illustrate transmitting, using the test circuitry, the second set of programming instruction to a second one of the plurality of ICs.

FIG 5 does not illustrate the transmitting is performed via the testing circuitry. The accompanying description discloses pathways 516, 518, and 520 provide for transmitting control signals from the EJTAG Master device to the EJTAG slave device (see Specification PAGE 8 LINES 5-20). Control signals are understood to be separate from a set of programming instructions as recited in the claims. Instead the accompanying description makes clear that the JTAG serial data pathways included in SoCs 502, 508,

and 512 but not illustrated in FIG 5 are utilized to transfer information such as program coddle and/or data from the NVM 504 to private external memories 506, 610 and 512 (see Specification PAGE 8 LINES 15-25).

V. CLOSING COMMENTS

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

Va. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a third action on the merits and are subject of a final office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

VI. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BRP/kp /KP/
July 26, 2010

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187